REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update to reflect latest changes in format and requirements. Editorial changes throughout. -les	01-09-19	Raymond Monnin

The original first sheet of this drawing has been replaced.

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REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

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DRAWING APPROVAL DATE
87-11-02

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, BIPOLAR,
TTL, DUAL MONOSTABLE MULTIVIBRATOR,
MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87711**

SHEET 1 OF 12

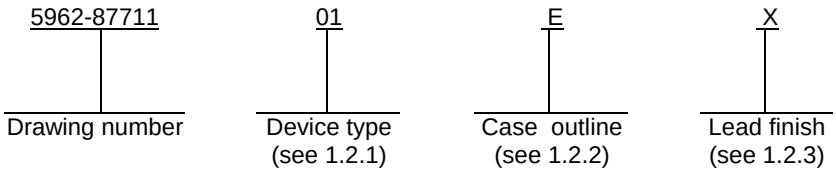
DSCC FORM 2233
APR 97

5962-E620-01

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54221	Dual monostable multivibrator

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range (V_{IN})	-1.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	440 mW 1/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case E	60°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case E	90°C/W
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH}) :	
Input A	2.0 V
Maximum low level input voltage (V_{IL}):	
Input A	0.8 V
High level output current (I_{OH})	-800 µA maximum
Low level output current (I_{OL})	16 mA maximum
Rate of rise or fall of input pulse (dv/dt):	
Schmitt input, B	1 V/s minimum
Logic input, A	1V/µs minimum
Input pulse width:	
A or B, $t_{W(IN)}$	50 ns minimum
Clear, $t_{W(CLEAR)}$	20 ns minimum
Clear-inactive-state setup time (t_{SU})	15 ns minimum

1/ Must withstand the added P_D due to short circuit test (e.g. I_{OS}).

External timing resistance (R_{EXT})	1.4 kΩ to 30 kΩ
External timing capacitance (C_{EXT})	0 pF to 1000 nF
Output duty cycle:	
R_{EXT} = 2 kΩ	67 percent maximum
R_{EXT} = 30 kΩ	90 percent maximum
Ambient operating temperature (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 -- List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms. The switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Positive going threshold voltage	V_{T+}	V_{CC} = 4.5 V Input B		All	1, 2, 3		2	
Negative going threshold voltage	V_{T-}	V_{CC} = 4.5 V Input B		All	1, 2, 3	0.8		V
High level output voltage	V_{OH}	V_{CC} = 4.5 V I_{OH} = -0.8 mA		All	1, 2, 3	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V I_{OL} = 16 mA		All	1, 2, 3		0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V I_{IN} = -12 mA		All	1, 2, 3		-1.5	V
Input current	I_I	V_{CC} = 5.5 V, V_{IN} = 5.5 V		All	1, 2, 3		1.0	mA
High level input current	I_{IH}	V_{CC} = 5.5 V, V_{IH} = 2.4 V	Input A	All	1, 2, 3		40	µA
			Input B, Clear				80	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IL} = 0.4 V	Input A	All	1, 2, 3		-1.6	mA
			Input B, Clear				-3.2	mA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V 1/		All	1, 2, 3	-20	-55	mA
Supply current	I_{CCH}	V_{CC} = 5.5 V	Quiescent	All	1, 2, 3		50	mA
			Triggered 2/	All	1, 2, 3		80	mA
Functional tests		See 4.3.1c		All	7			
Propagation delay time, A to Q	t_{PLH1}	C_L = 15 pF R_L = 400Ω C_{EXT} = 80 pF R_{EXT} = 2 kΩ V_{CC} = 5 V (See figure 4)		All	9		70	ns
				All	10, 11		91	
Propagation delay time, A to $\overline{Q}$	t_{PHL1}			All	9		80	ns
				All	10, 11		104	
Propagation delay time, B to Q	t_{PLH2}			All	9		55	ns
				All	10, 11		71.5	
Propagation delay time, B to $\overline{Q}$	t_{PHL2}			All	9		65	ns
				All	10, 11		84.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Propagation delay time, clear to $\overline{Q}$	t_{PLH3}	C_L = 15 pF R_L = 400Ω C_{EXT} = 80 pF R_{EXT} = 2 kΩ V_{CC} = 5 V (See figure 4)		All	9		40	ns
				All	10, 11		52	ns
Propagation delay time, clear to Q	t_{PHL3}			All	9		27	ns
				All	10, 11		35.5	ns
Pulse width, A or B to Q or $\overline{Q}$	$t_{W(out)}$	C_L = 15 pF R_L = 400Ω T_A = +25°C V_{CC} = 5 V (See figure 4)	C_{EXT} = 80 pF R_{EXT} = 2 kΩ	All	9	70	150	ns
			C_{EXT} = 0 pF R_{EXT} = 2 kΩ	All	9	20	50	ns
			C_{EXT} = 100 pF R_{EXT} = 10 kΩ	All	9	650	750	ns
			C_{EXT} = 1 µF R_{EXT} = 10 kΩ 2/	All	9	6.5	7.5	ms

1/ Not more than one output should be shorted at a time and the duration of the short circuit condition should not exceed one second.

2/ This test is guaranteed if not tested to the parameters specified in table I.

Device types	01
Case outlines	E
Terminal number	Terminal Symbol
1	1A
2	1B
3	$1\overline{CLR}$
4	$1\overline{Q}$
5	2Q
6	$2c_{ext}$
7	$2R_{EXT}/c_{EXT}$
8	GND
9	2A
10	2B
11	$2\overline{CLR}$
12	$2\overline{Q}$
13	1Q
14	$1c_{EXT}$
15	$1R_{EXT}/c_{EXT}$
16	V_{CC}

FIGURE 1. Terminal connections.

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊓**
H	↓	H	⊓	⊓**
↑*	L	H	⊓	⊓**

H = High level voltage.
L = Low level voltage.
X = Irrelevant.
⊓ = One high level pulse.
⊔ = One low level pulse.
↑ = Low to high level transition.
↓ = High to low level transition.

* This condition is true only if the output of the latch formed by the two NAND gates has been conditioned to the logical "1" state prior to CLR going high. This latch is conditioned by taking either A high or B low while CLR is in the inactive state.

** Tested under subgroup 9.

FIGURE 2. Truth table (each monostable) .

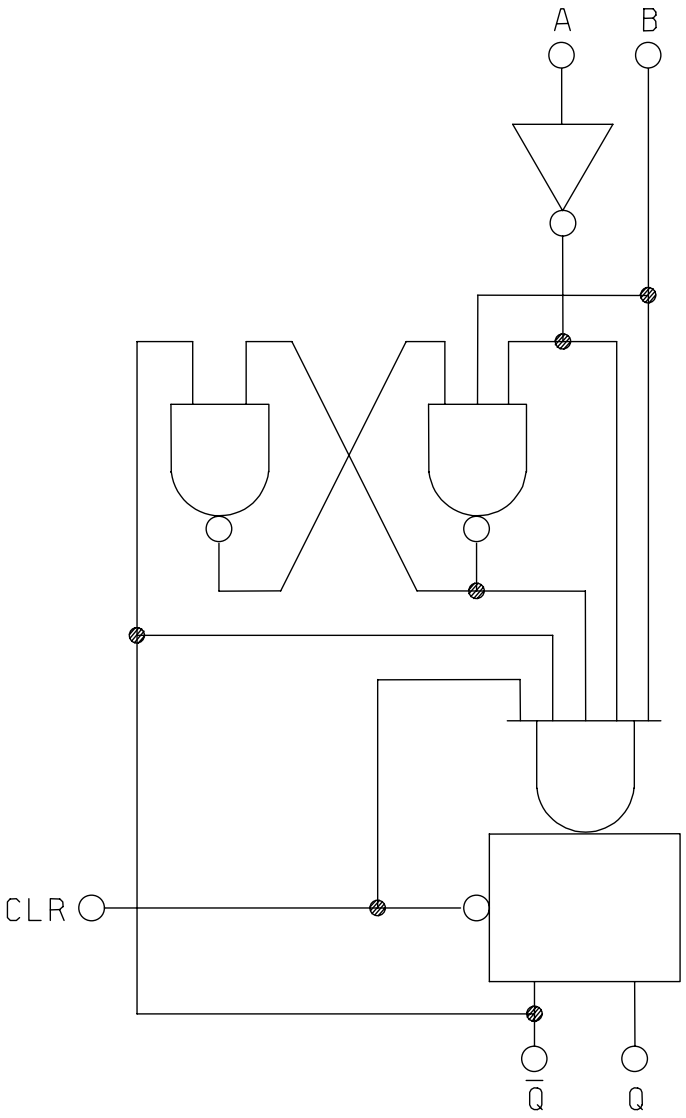


FIGURE 3. Logic diagram (one-half of the device) .

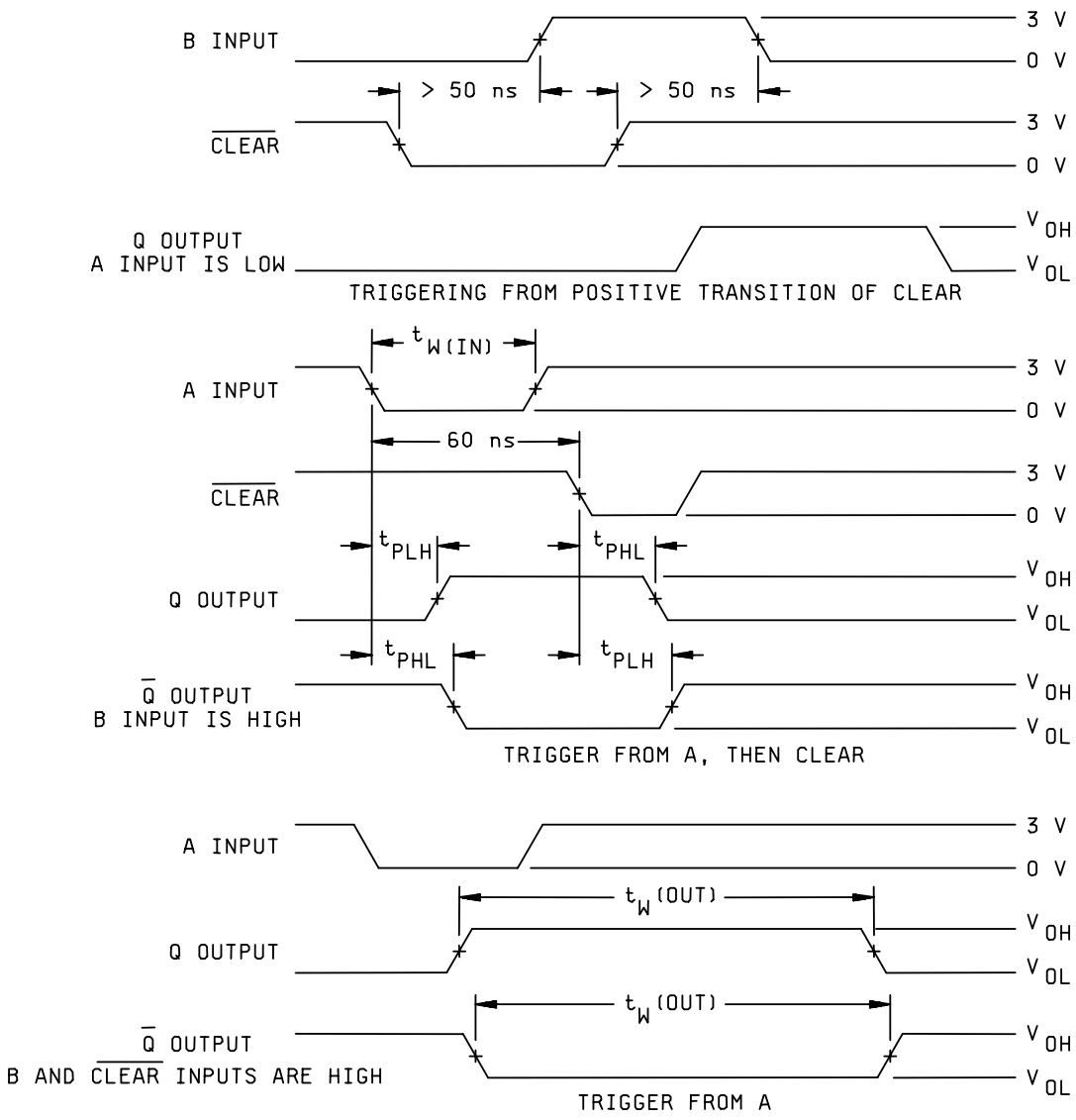
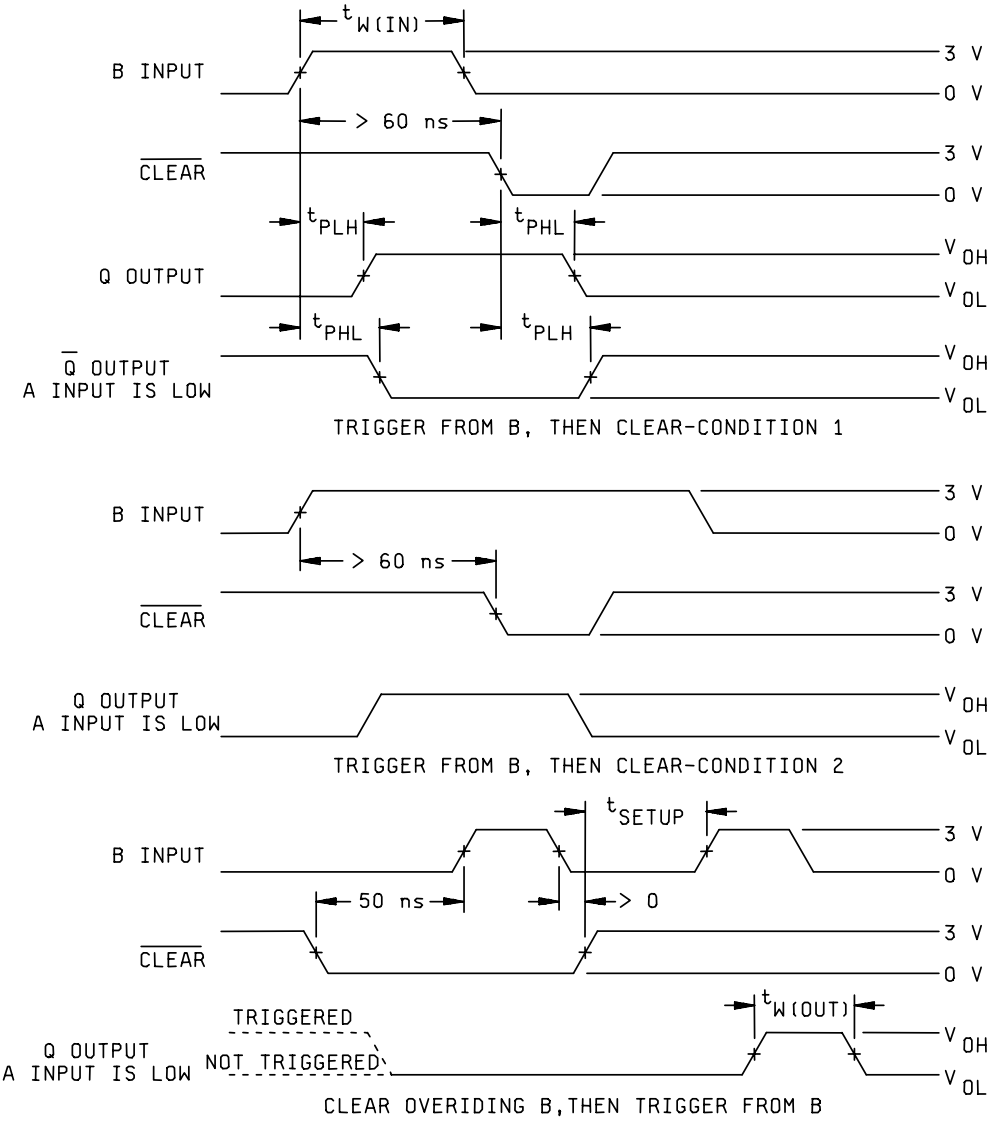


FIGURE 4. Switching waveforms.



NOTES:
1. Input pulses are supplied by generators having the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$, $t_r < 7$ ns, $t_f < 7$ ns. Duty cycle = 50% ±50%.
2. All measurements are made between the 1.5 V points of the indicated transitions.

FIGURE 4. Switching waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 tests shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-09-19

Approved sources of supply for SMD 5962-87711 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8771101EA	01295 58625	SNJ54221J SL54S221/BEA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, Tx 75243 POC U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493
58625	LANSDALE SEMICONDUCTOR INC 2929 South 48th ST Tempe, AZ 85282